RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2018

FIRST YEAR [BATCH 2018-21]

Date : 14/12/2018 **COMPUTER SCIENCE (Honours)**

Time : 11 am – 3 pm Paper : I Full Marks : 75

(Use a separate Answer book for each group)

Group – A

Answer **any one** question from **Question Nos. 1 & 2**: 1 X 5

1. a) Write an algorithm for conversion of decimal integers to integers in radix R, where R< 10. 4
   b) State any two characteristics that an algorithm should have. 1
2. a) Perform the following using 2's complement method: $(1011.11)_2 - (101.01)_2$ 2
   b) Perform the following conversion : $(0.9512)_{10}$ to its equivalent octal number. 1
   c) Convert the following pattern, in Gray code format, to its equivalent binary code: $(1011101)_G$ 2

Answer **any two** question from **Question Nos. 3 & 6**: 2 X 10

3. a) Define prime implicant. 1
   b) Obtain the dual of the following function. $\bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$ 1
   c) Realize X-OR logic using NAND and NOR logic respectively. 1.5+1.5
   d) Define minterm and maxterm in connection with a Boolean expression. Express the following Boolean function as a sum of minterms : F(x,y,z) = x+yz (1+1)+3

4. a) State and prove the distribution law for Boolean algebra. 2+2
   b) State the limitations of 'Karnaugh Map'. 2
   c) Draw the Binary Decision Diagram for the following function.
   $f(x_1,x_2,x_3) = \bar{x}_1\bar{x}_2\bar{x}_3 + x_1x_2 + x_2x_3$ 4
5. a) Write down the connectives of propositional logic. 2
   b) Define tautology & contingency. 2+2
   c) Define CNF and DNF. 2+2

6. a) For a code to be self-complementing what must be the sum of all its weights and why ? 2
   b) Discuss on the demerits of machine language use in connection with an application development. 2
   c) What is a non-weighted code ? Give two example of the same. 1+1
   d) A 12-bit Hamming code word contains 8-bits of data. What is the original 8-bit word if the 12-bit read out as follows ? 1010 1001 1101 3
   e) Determine the possible base in the following operation.
   23+44+14+32=223 1

Group – B

Answer **any five** questions **Question Nos. 7 & 14**: 5 X 10

7. a) Design a logic circuit to convert a 4-bit binary code to its equivalent Gray code format. 4

   b) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable input and one 2-to-4 line decoder and explain its operation. 4+2

8. a) Mention the main characteristics of Von Neumann architecture. 2

   b) Show how Booth's multiplication algorithm performs fewer addition and subtraction than a straight forward algorithm. perform $(5)_{10} \times (2)_{10}$ using Booth's algorithm. 2+3

   c) Design a 2-bit asynchronous down counter using positive adge triggered D flip-flop. 3

9. a) Represent $(59.125)_{10}$ in IEEE single precision format. 3

   b) Implement the operation of a 2-input NAND gate using suitable multiplexer. 4

   c) Realize a J-K flip-flop using a D flip-flop. 3

10. a) What is an addressing mode ? 2

    b) Briefly state the differences between a RISC architecture and a CISC architecture. 2

    c) Design a 3-bit universal shift register using the following mode of operation table. 4

s_1	s_1	Operation
0	0	Parallel Load
0	1	Shift Left
1	0	Shift Right
1	1	No Change

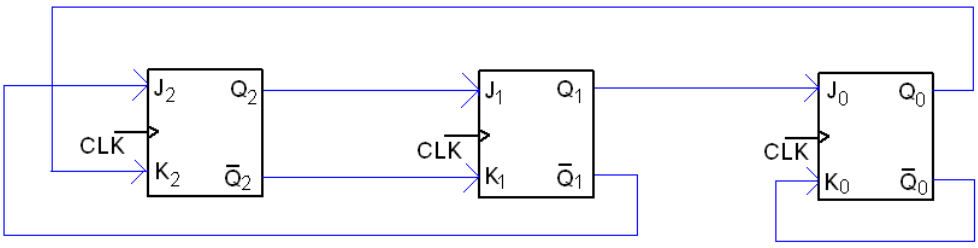
    d) What is a Johnson's Counter ? 2

11. a) Design a 128×8 RAM using 64×8 RAMs and other necessary combinational circuit. 3

    b) What do you mean by Content Addressable Memory (CAM) ? 2

    c) How does a Master-Slave flip-flop solve the problem caused by the race around condition ? 2

    d) Explain race around condition. 3



The above synchronous sequential circuit built using JK flip flops is initialized with $Q_2Q_1Q_0 = 000$. Find out the state sequence for this circuit for the next three clock cycles.

12. a) What does the hardwired control generator consists of ? What is the role of a control word in a microprogrammed control unit ? 3

    b) A computer has 256 MB of main memory. The 1 MB cache uses direct mapping with block size of 16 words. How many bits are there in tag, line and word fields of the address format. 3

c) State the modes of operation that are followed at the time of direct memory access. 2

d) ' A decoder with an enable input is called a demultiplexer' — Justify. 2

13. a) What is a tri-state device ? Briefly state its importance. 4

b) What do you mean by vectored interrupt ? Give proper example. 2

c) Design and implement the logic circuit of a BCD adder. 4

14. a) What is bus arbitration ? What is drawback of daisy chaining ? How can it be reduced ? 4

b) Discuss on different cache write policies. 3

c) Design a combination logic circuit to produce 2's complement of a 3-bit binary number. 3

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